Superconducting circuits with silicon technology

- *Scientific context*

Quantum engineering is at the heart of what is now called the second quantum revolution. The issue is no longer to demonstrate the validity of quantum mechanics but to imagine and elaborate objects and circuits whose properties and functionalities are driven by quantum mechanics. An important expected outcome is the development of a new technology for communication and information based on quantum elements such as quantum bits (qubits). In this quest, solid state qubits appear as very good candidates especially because of their better scalable potential compared to their optical counterparts.
Nowadays the most advanced technology is based on superconducting qubits which include tunnel Josephson junctions coupled to superconducting resonators (transmon) [Devoret2013]. The properties of a transmon qubit depend strongly on two competing energies. The charging energy E_c and the Josephson energy E_J. The transmon qubit operates in a regime where the ratio E_c/E_J is large. In that case, the qubit has a reduced anharmonicity but is almost insensitive to charge fluctuations which reduces drastically decoherence.
The manipulation and the read-out of the qubit states require micro-wave elements in the GHz range set by the energy spectrum of the qubits. In most of the realizations, microwave circuits are implemented by superconducting resonators capacitively coupled to the qubit ; And the Josephson energy controlled by placing two Josephson junctions in superconducting loop coupled to a flux biasing line that requires DC current of the order of a mA. In the prospect of building large-scale qubit architectures – fault-tolerant surface-code architectures are currently expected to require millions of qubits – the associated energy to supply the bias circuitry is a serious issue.
Recently a new type of transmon has emerged and is based on Josephson junctions made from semiconducting InAs nanowires [Larsen2015, deLange2015]. In that case, the shunted capacitance must be engineered on chip because the intrinsic S/D shunting capacitance is very small. For superconductor / semiconductor / superconductor (S-Sm-S) junctions, the electrostatic gate changes the transmission of the channel and results in a modulation of the Josephson energy. Such new gate tunable transmons are called gatemons and offer new possibilities for complex architectures.

The objective of this project that goes beyond the PhD thesis, is to fabricate a silicon GATEMON in a fully CMOS compatible and scalable technology. It will include the realization of silicon transistors with superconducting S/D contacts coupled to superconducting microwave resonators.

This new superconducting qubit will be based on a silicon transistor with superconducting source and drain contacts. The superconducting contacts will be fabricated from superconducting silicides (PtSi T_c ~1 K) or boron doped Silicon (Si:B) that can be superconducting using laser doping/annealing. In the case of silicides, the goal is to control the metal/semiconductor solid state reaction in order to obtain the good superconducting phase as close as possible to the transistor channel. Another promising silicide (V_3Si T_c~15K) will also be investigated. For Si:B, the issue is to control the laser doping/annealing on silicon on insulator (SOI) and on pre-existing devices without damaging them. The superconducting resonators will also be implemented from the same materials and a careful and systematic study of their performance will be performed.

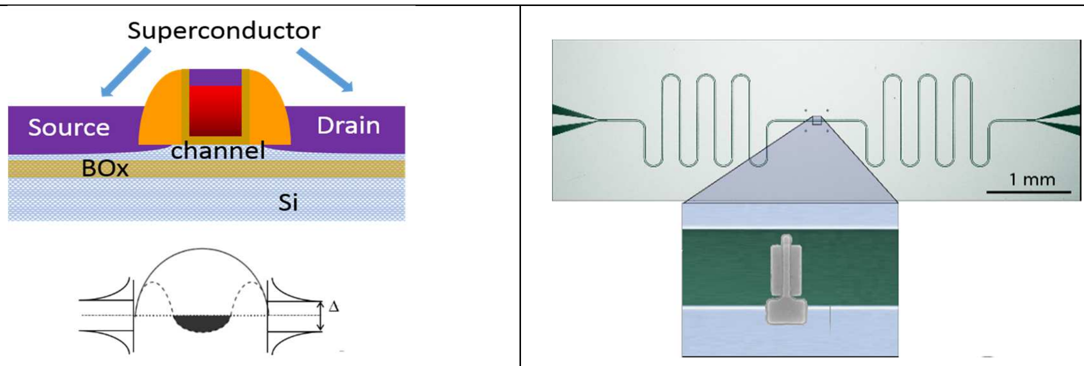

Fig. 1: Left: Schematics of a superconducting MOSFET and simplified energy diagram with the superconducting gap Δ. Right: Possible realization of a silicon gatemon inspired by [Wallraff2004]. The SEM image is an actual MOSFET realized at the LETI. In this scheme, the gate of the transistor is connected to the central part of the resonator.

- *Originality and innovative aspects of the project*

The first originality of the project is that it has been elaborated to use the existing silicon technology to realize quantum objects that are, at least for the moment, far away from the business core of this industry. Even the most technologically demanding task on laser annealing fits along the road map towards 3D integration. The potential scalability and low variability of the silicon technology is such that progress towards more complex architectures addressing quantum computation issues will be very fast. Once the silicon gatemon operation is demonstrated, the silicon technology will rapidly fill the gap with the commonly used aluminum based technology for tunnel junction superconducting qubits.

The second originality of the project is that the required technological developments will find, to some extent, their implication in the silicon industry. Indeed, the reduction of the access resistance for commercial transistors is an important issue for the semiconducting industry as they contribute non-negligibly to the power consumption and to Joule heating. Any step towards a gain in lowering the contact resistance and/or a better understanding of a metal/semiconductor interface will have its own interest beyond the objectives of this project.

- *Thesis objectives and research program: strategy, methods and techniques, expected timing*

The thesis program will mostly be focused on the realization and study the low temperature properties of MOSFETs with superconducting PtSi silicide S/D contacts. The PhD work will start at the CEA-LETI in order to implement MOSFET with superconducting silicides. This will include first the fabrication and characterization of the PtSi superconducting thin films. Starting from the deposition of a platinum film on silicon, the conditions of annealing temperature and time will be studied to grow the right PtSi phase and to optimize the critical temperature which is expected around 1K. To obtain the right parameters, systematic x-rays and low temperature resistive behavior will be performed. In a second phase, the characterization of interface transparency between the silicide and (doped) silicon will be addressed. Test structures like TLM and cross bar Kelvin resistance will be fabricated and measured at low temperature. The parameters will be optimized in order to reach a transparency larger than 0.1 corresponding to a contact resistance of the order of $10^{-8}\ \Omega\ .\ cm^{-2}$ which is the level reached in the past by the LETI with the same material in the fabrication of Schottky barrier MOSFET [Poiroux2009]. The recipe for the lowest contact resistance will be adapted and optimized and integrated to the fabrication of nanoMOSFET using the FDSOI technology at LETI. The devices will be as short as possible down to 50 nm and rather large up to 1 µm to favor Josephson coupling and reduce charging energy.

Finally, samples with superconducting silicon Si:B S/D contacts may also be available but the fabrication goes beyond the PhD program. Such devices will be fabricated within a collaboration between INAC, LETI and C2N-Orsay.
In parallel, superconducting resonators will be fabricated and their performance characterized at low temperature. Keeping in mind scalability, PtSi or TiN material will be used and various supporting environment (bulk Si, SOI, SiN) will be tested.
By the end of the PhD thesis, should first devices including both a superconducting MOSFET and superconducting resonator be ready and quantum coherent manipulation of quantum states be performed at low temperature.
The first easily realizable objective is to measure, at low temperature, a superconducting MOSFET independently of the contact transparency. The achievement of Josephson junction in the strong coupling regime, is the target but very nice scientific investigations can be pointed out even in the case of weak coupling regime. Those may appear first and will ensure intermediate results to be published. In that case the charging energy will overcome the Josephson energy. Spectroscopic measurements of the silicon quantum dot charge states will be performed with an unprecedented energy resolution thanks to the strong discontinuity at the superconducting gap edge. In addition, turnstile effect will then be demonstrated and will correspond to DC current under RF modulation of the gate.

	Year 1	Year 2	Year 3
Time sharing	LETI (80 %) PHELIQS (20%)	LETI (30 %) PHELIQS (70 %)	LETI (10 %) PHELIQS (90 %)
Main activities	• Thin film growth PtSi, V_xSi • Test structures: Fab & Low temp. studies • Supercond. Resonators: Fab & low temp. studies	• PtSi & V_XSi MOSFET: Fab & Low temp. studies • Supercond. Resonators: cont'd	• PtSi MOSFET: Low temp. studies cont'd • Supercond. Silicon based MOSFET: Low temp. studies

To accomplish his PhD work, the candidate will be co-supervised by François Lefloch (main) at PHELIQS and by Fabrice Nemouchi at LETI. The project will also benefit from collaborations with INEEL (O. Buisson and N. Roch) to investigate and understand the frequency response of the resonators. For superconducting MOSFETs in the weak coupling regime the study will follow the results obtained by H. Courtois and C. Winkelman on devices comprising gold quantum dot with superconducting aluminum electrodes.
The candidate will have full access to the LETI facilities to lead the project. The cost associated with technological developments at LETI will be covered by internal resources. For low temperature measurements, the candidate will benefit from dedicated cryogenic experimental setups at PHELIQS. Any additional fabrication steps like contacting preformed MOSFETs or ebeam lithography will be done at the PTA.

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