Non-volatile MRAM-based asynchronous ASIC study and design

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PhD may follow: Yes

Summary :

Preliminary training for a Ph. D objective.

Since microelectronics limits are currently quite reached, several methods trends to push them further. The objective of the training is to investigate several ways combining different advantages of microelectronics very advanced processes such as FD-SOI (Fully Depleted on SOI substrate) and advanced non-volatiles memory processes such as MRAM (Magnetic Random Access Memory). This would be combined with asynchronous design method that enable to optimize some applications such as ultra low power for instance.

This training would be led by the "ASIC design" dynamic group within SPINTEC lab in CEA Grenoble. This lab is specialized in the spintronics: study, nano-fabrication and use of magnetic tunnel junctions. The analog design environment is the Cadence suite and the digital environment is Synopsys. The training can be adapted to the candidate skills.

Requested skills :

Analog and digital ASIC design. Use of Cadence Schematic Composer / Virtuoso tools. VHDL and/or Verilog language. SoC.