Non-volatile digital integrated circuit test and characterization

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PhD may follow: Yes

Summary :
Several version of a digital integrated circuit have been designed and fabricated. The objective of the training is to understand the circuit's behavior and then to test and characterize it.

Full description :
In the framework of a collaboration between 2 CEA's laboratories LCM (Memory Device Lab) and Spintec (mixed research unit between CEA/CNRS/Univ. Grenoble), an hybrid CMOS/MRAM (Magnetic Random Access Memory) circuit has been designed and fabricated. The MRAM is an emergent non-volatile technology, based on the single device called MTJ (Magnetic Tunnel Junction). The objective of this training is first of all to understand the MRAM technology,to control the behavior of this circuit and then to test and characterize it. This circuit is composed of simple test structures (! transistor / 1 MTJ) and several versions of a digital filter. The required skills are good knowledge in integrated circuit design and some knowledges in programming. Indeed, tests will be performed using an industrial tester controlled by a graphical interface.

This training is suppose to lead to a Ph. D in the domains of non-volatiles integrated circuit design and micromagnetic simulations that would enable to anticipate and analyze the MTJ behavior according to several fabrication criteria.

Requested skills :
Integrated circuit design
Programming
Test