Simulation, modelling and characterisation of quasi-ballistic transport in nanometer sized field effect transistors: from TCAD to atomistic simulation

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Abstract: In this paper, we review and contrast some computational methodologies to investigate charge transport in low dimensional materials and devices. This includes ultra-scaled MOS devices as well as nanowires-based field effects transistors or carbon nanotubes-based emerging devices. After presenting the context of nanodevice simulation, the focus will be made on the limits for ballistic transport in these several types of nanodevices.

Keywords: charge transport; transistor simulation; Monte Carlo; tight-binding; non equilibrium green functions; Kubo approach; Landauer-Büttiker method.

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Biographical notes: Stephan Roche received the MSc from Ecole Normale Supérieure de Lyon (1993) and PhD Degree from the University of Joseph-Fourier (Grenoble) in 1996. After working at Tokyo University (Japan) and Valladolid University (Spain) as an EU post-doc, he was appointed as an Assistant Professor at University Joseph-Fourier in 2000. He joined the Commissariat à l'Energie Atomique (CEA-INAC), as a research staff member in 2004. He has a broad experience in studying quantum transport and computational modelling of low dimensional systems and complex materials. His main achievements are in the fields of carbon nanotubes, DNA, 2D graphene, semiconducting nanowires, and π-conjugated systems. During the last decade, he and his co-workers have developed various novel real space order N methods for the computation of transport coefficients either within the Kubo-Greenwood or Landauer-Büttiker formalisms both in equilibrium and non-equilibrium conditions. He has authored or co-authored about 80 papers (20 PRL). He has supervised research activities in computational nanosciences within the CEA ChimTronique programme. In 2008, he was awarded the Friedrich Wilhelm Bessel prize from the Von-Humbolt Foundation.

Thierry Poiroux received his MSc and PhD respectively from Ecole Centrale Paris (1995) and University of Nantes (2000). His PhD work was carried out at LETI and Matra MHS on plasma process-induced damage. He joined LETI as a Research Staff Member in 2000. He has been involved in partially and fully-depleted SOI process integration and compact modelling. From 2002 to 2007, he worked on advanced device architectures. He was in charge of multiple-gate device modelling and involved in planar double gate process integration. Since 2007, he has been working on graphene, which is a promising material for the beyond CMOS era. He has authored or co-authored about 70 papers and communications.

Gilles Lecarval received the Diploma of Telecommunication Engineer, in 1985 from the National Telecommunication School. In 1985 he also received the (DEA) from the Polytechnics Institute of Grenoble (INPG), specialisation in Microelectronics. From 1985 to 1989 he was at LETI to prepare a PhD on the physics of EPROM writing mechanisms involving Hot Carrier Transport Mechanisms. After obtaining his PhD, he was hired at LETI as device engineer for the development of non-volatile memories. In 1993 he was the co-founder of a the TCAD group, for this date he has been involved in the development of new TCAD activities (methodology for calibration for TCAD tools, parasitic interconnect modelling including low and high frequencies up to 40GHz, atomistic simulation, modelling of single-electron devices, and more recently modelling of new materials for TCAD such as strained silicon, germanium… with a specially attention to the analysis of non-stationary, quasi-ballistic and quantum effects in MOS devices). From 1999 he has been member of the ITRS Working Group for TCAD. He is author or co-author of about 50 papers.

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1 Introduction: State of the art of computational approaches for nanodevices simulation

The race for downscaling CMOS technology is about to reach an insurmountable wall: the nanoscale limit. For decades, the reduction of the silicon channel has been concomitant with improved field effect transistor efficiency and enlarged massive device integration [1]. Along the way, each new node has witnessed the integration of new materials and process steps to achieve the objectives of the ITRS roadmap of semiconductors industries. This has included for instance the integration of high-κ dielectrics, the archetype of which is hafnium oxide, that have been shown to significantly reduce can gate leakage. Mechanical strain applied in the channel and substrate orientation was also found to improve carrier mobility, as well as the use of alternative device geometries, such as double-gated devices. However today, the true behaviour and limits of the high-κ gate dielectric and the double-gate geometry on silicon channel mobility still need to be accurately quantified. This requires advanced simulation methods that go beyond classical tools. Nowadays, major advances in the development of first principles approaches allow for a deeper analysis of material

properties at the nanoscale (such as energy band gaps alignment between different materials, etc.). Based on these achievements, a continuous flow of innovation could be developed to bridge ab initio up to Technology Computer-Aided Design (TCAD) models, essential to provide semiconductors industries a competitive advantage for a true device development and optimisation in terms of time-cycle and wafer-costs.

Several classes of quantum and transport solvers are nowadays available or emerging. Monte Carlo Solvers [2] model charge transport via the semi-classical Bloch-Boltzmann equation, which is solved in a stochastic way, using a classical description of the propagating electrons but a quantum description of their energetic. More advanced quantum-transport solvers are based on the so-called Non-Equilibrium Green Function Method (NEGF), in which carrier transport is treated using the full quantum Green function formalism [3,4]. Both approaches are however still in the development phase, and no ready-to-use industrial solutions are available so far to meet the requirements of the 32 nm node and beyond. From the point of view of technology development support, the Monte Carlo simulators should be able to provide reliable electrical results on regular basis for 32 nm MOS devices. However the needs for full-band Monte-Carlo codes together with band structure solvers that account for strain and are capable of dealing with new materials remain unsettled. Some commercial 3D Schrödinger solvers [3] using NEGF solvers can already be used to model ballistic quantum transport in advanced devices with strong transverse confinement. However, they do not include any inelastic scattering mechanism, and thus are not suitable for the calculation of transport properties in the 32 nm node devices and near future nodes.

In this paper, we will present different computational approaches developed at CEA (MINATEC-Leti and INAC) to simulate charge transport in ultra-scaled MOS devices as well as nanowires-based field effects transistors or carbon nanotubes-based emerging devices. Some details about the methodologies will be pinpointed, and the focus will be made on the limits for ballistic transport in these several types of nanodevices. Indeed, one of the outcomes of size reduction is to benefit from reduction of scattering sources that drive the energy dissipation of the device and lower corresponding performances.

2 Some scattering mechanisms limiting the ballistic transport in ultimate MOSFETs

2.1 Introductive remarks

Aggressive scaling of complementary metal-oxide-semiconductor (CMOS) technology is required so as to meet the International Technology Roadmap of Semiconductors projects in terms of circuit efficiency and device performance. However, to circumvent the downscaling difficulty and extend the lifetime of conventional silicon technology, novel architectures as well as new materials are currently explored. Among the promising candidates, thin-film strained silicon-on-insulator (s-SOI) nMOSFETs using a $TiN/HfO_2/SiO_2$ gate stack appear to be a good avenue for the upcoming technological nodes [5]. Indeed, the use of a high-κ dielectric like HfO_2 reduces the gate leakage current, while substrate induced biaxially tensile strain enhances the electron mobility (by about 100% using a stress of 1.4 GPa). However, the understanding of the electronic transport in such devices is still rather incomplete. Especially, there is a lack of investigation about two major issues that degrade charge transport, namely,

i Coulomb centres in the gate stack near the HfO_2/SiO_2 interface (*via* the so-called remote Coulomb scattering, RCS)

ii the scattering with the fluctuations of the SiO_2/(s)SOI interface (surface-roughness scattering, SRS).

These two scattering mechanisms, RCS and SRS, are known to limit the mobility at low and high electron sheet density respectively. Therefore, modelling and simulation tools are highly desirable to serve as guide-lines for explaining and improving the electrical behaviour of these devices.

2.2 Surface roughness scattering

In recent years, many groups have reported both large electron and hole mobility improvements in s-SOI MOSFETs over their conventional SOI architectures [6–8]. In order to explain the effect of strain on the electron effective mobility in biaxially strained silicon inversion layers, we have carried out an experimental and theoretical analysis via atomic force microscopy measurements and Kubo-Greenwood mobility calculations. The Kubo-Greenwood formulation used in this work comes from the linearisation of the Boltzmann transport equation. Multiplying the Boltzmann equation by the carrier velocity and the momentum relaxation time, summing over the bands or valleys, and integrating over the wave vector **k**, we can extract the mobility from the current density [9]. Standard (001) SOI and s-SOI substrates (both with 145 nm buried oxide) have been used for the AFM analysis. For both wafer types, the film thickness is equal to 15 nm. s-SOI substrates have been processed using a relaxed $Si_{0.2}Ge_{0.8}$ virtual substrate as a template. The AFM image (cf. Figure 1 – by courtesy of O. Faynot from LETI/D2NT/LDI) are digitised, thus giving an image lattice $h(\mathbf{R})$ on an $N \times N$ two-dimensional mesh, where N is the number of surface sites. Figure 2 illustrates the normalised height distribution functions for SOI and s-SOI films. Then, the surface morphology is analysed through the calculation of the roughness amplitude, Δ, which is a key parameter to characterise the SR. Over different scan sizes, 200×200 nm^2, 500×500 nm^2 and 2.5×2.5 μm^2, it is found that Δ in s-SOI is smaller than Δ in SOI. A ratio $\Delta_{s\text{-}SOI}/\Delta_{SOI} \approx 1.5$ is obtained when we average over the three scan areas [10]. To gain some physical insight concerning the strain dependence of the surface morphology, some important statistical properties of the sequence $h(\mathbf{R})$ have been studied.

Figure 1 AFM image (200×200 nm^2) of s-SOI substrate. The lattice mismatch in the s-SOI film is 0.8% (see online version for colours)

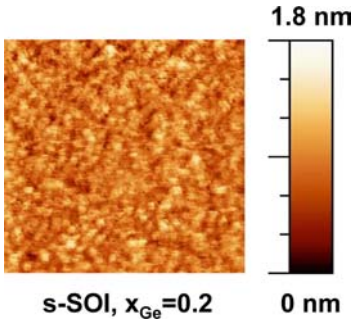
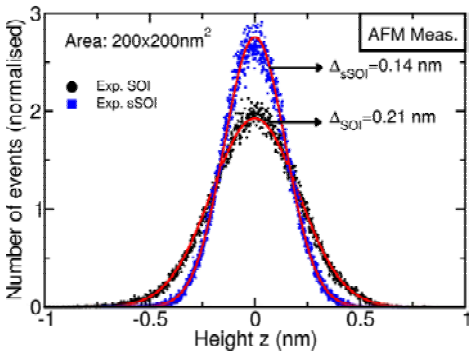


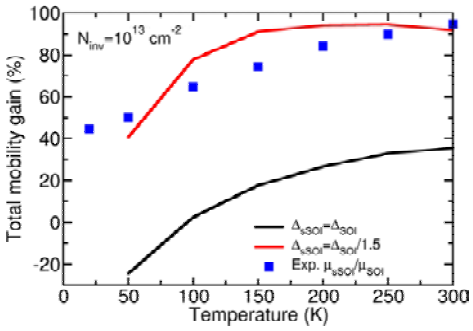
Figure 2 Normalised height distribution functions for SOI and s-SOI (x_{Ge} = 20%) films (see online version for colours)



The so-called height-height correlation function has been calculated. It is directly related to the autocorrelation function and therefore to the power spectrum density (PSD) of the surface via Fourier transform. The PSD is useful since it enters the calculation of the momentum relaxation time relative to SR scattering [11] and thus is linked to the SR limited mobility, μ_{SR}. The effective mobility is calculated using the Kubo-Greenwood formulation within the framework of a two-dimensional electron gas [12]. The quantisation of energy levels and the associated wave functions result from a self-consistent resolution of the 1D Schrödinger-Poisson equations in the confinement direction. In order to highlight the physical mechanism responsible for the mobility enhancement at high electron density N_{inv}, we have calculated the ratio between the mobility in s-SOI over the one in SOI as a function of the temperature for $N_{inv} = 10^{13}$ cm^{-2}. Using the same roughness parameters for describing the SOI/SiO_2 and s-SOIs/SiO_2 interface the disagreement between the theoretical and the experimental mobility gain is maintained over the whole temperature range (Figure 3).

On the other hand, using a reduced roughness amplitude for the mobility calculation defined by the ratio $\Delta_{s\text{-}SOI}/\Delta_{SOI} \approx 1.5$ (AFM results), a better agreement with the experimental data is noticed. This demonstrates that the mobility gain at a high electron density is mainly due to the smoothness of the s-SOI/SiO_2 interface.

Figure 3 Total mobility gain as a function of the lattice temperature using different values of $a = \Delta_{SOI}/\Delta_{s-SOI}$. The closed squares are the experimental measurements (from Leti). Solid line: a = 1; dashed line: a = 1.5 (see online version for colours)



2.3 Remote Coulomb scattering

In this section, another scattering mechanism limiting the low field mobility in MOSFETs with TiN/HfO_2/SiO_2 gate stack is investigated. Indeed, a recent experimental investigation of electron and hole mobility in devices integrating both a high-κ dielectric (HfO_2) and a metal gate (TiN) has shown the prominent effect of remote-Coulomb-scattering (RCS) due to a large amount of charges located at the HfO_2/SiO_2 interface inducing a significant degradation of mobility [13]. Then, to have a better understanding of the role played by Coulomb centres trapped in the gate stack, we have developed a physical model of RCS. A usual Metal Insulator Semiconductor (MIS) geometry is considered. The gate dielectric is composed of a high-κ film (HfO_2) with a SiO_2 interfacial layer and insulates the gate electrode from the Si substrate. As previously, the quantisation of energy levels and the associated wave functions result from a self-consistent resolution of the 1D Schrödinger-Poisson equations in the confinement direction. Then, Green's function for the Poisson equation is derived to find the perturbation induced by a point charge seen by the inversion layer electrons [14]. In Figure 4, we plot the perturbing potential induced by a charge e located at various distances z_0 away from the HfO_2/SiO_2 interface. As expected, the inversion layer electrons will be less sensitive to the perturbation induced by the charge if it is moved away from the HfO_2/SiO_2 interface.

Figure 4 Unscreened Coulomb scattering potential of a point charge calculated at different positions z_0 inside the high-κ dielectric. The impact of the charge in the channel is reduced when it is moved away from the HfO_2/SiO_2 interface

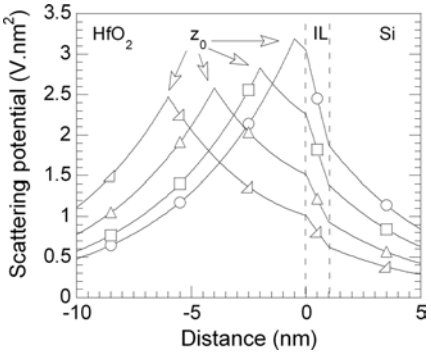
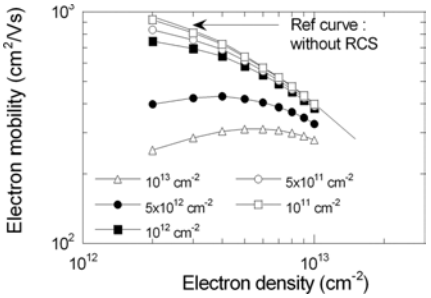
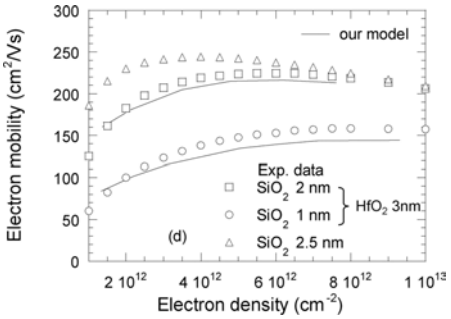


Figure 5 Electron mobility as a function of the electron density. The mobility is calculated for various charge densities N_{fix} (1013 cm^{-2} down to 1011 cm^{-2}) located at 0.5 nm from the HfO_2/SiO_2 interface



Then, the momentum relaxation time as well as the low-field electron mobility has been calculated using the same Kubo-Greenwood formulation. Figure 5 shows the electron mobility calculated in SOI MOSFET device with and without charge density located at the HfO_2/SiO_2 interface. We can observe that the mobility degradation may be lower by 10% if the charge density $N_{fix} \leq 10^{11}cm^{-2}$. However, for charge densities close to 5×10^{12} cm^{-2} a degradation mobility of around 60% is expected at low electron density in the inversion layer. Then, the model has been compared to experimental data. The simulated gate stack includes 1–2 nm interfacial SiO_2 oxide, 3 nm HfO_2 and a metal gate in order to reproduce the same geometrical dimensions than the experimental one. Figure 6 shows the experimental mobility without HfO_2 integration (open triangle) – our reference curve – and with HfO_2 integration including the two thicknesses of interfacial SiO_2 layer. The theoretical RCS-limited mobility corresponding to an interfacial SiO_2 layer $t_{SiO_2} = 2$ nm has been added – using the Mathiessen rule – to the experimental reference curve. We can observe in Figure 6 that the resulting mobility well reproduces the experimental mobility over all the electron density range for a charge density fixed to $N_{fix} = 1 \times 10^{13}$ cm^{-2}. Now, using thinner SiO_2 interfacial layer (1 nm) the good agreement is maintained with charge density values with $N_{fix} = 2 \times 10^{13}$ cm^{-2}. The slight difference of adjusted N_{fix} values between SiO_2 IL of thickness 1 nm and 2 nm suggests that the amount of charge at the HfO_2/SiO_2 interface may change with the deposited HfO_2 layer.

Figure 6 Calculated (solid lines) vs. extracted (open symbols) experimental mobility for MOSFETs with HfO_2/SiO_2 gate stack at 300 K. The calculated mobility μ_{RCS} added to our SiO_2/TiN reference mobility well reproduced the mobility degradation



Finally, these scattering mechanisms are now implemented in the quantum-corrected Monte-Carlo simulator [15] ('Monaco' developed at Institut d'Electronique Fondamentale-Orsay) in order to investigate their impact on the electrical performances of short-channel SOI MOSFETs devices.

2.4 Electrical characterisation of quasi-ballisticity

On the other hand, to characterise properly the transport in ultra-short devices, the concept of mobility may no longer be appropriate and the quasi-ballistic nature of the transport needs to be accounted for. In order to characterise the quasi-ballisticity of experimental devices, simple analytical drain current models are required as well as methodologies for practical quasi-ballistic parameter extraction. The approximations

required to obtain a tractable analytical model have to be carefully validated by advanced numerical simulation tools.

A model of quasi-ballistic current in nanoscale transistors has been proposed in Rahman and Lundstrom [16], using an approach similar to the ballistic current modelling presented in Natori [17]. This drain current model is defined in the effective mass approximation as the sum of the currents on all the energy sub-bands, determined at the so-called virtual source. The virtual source is the point in the channel corresponding to the top of the potential barrier. For a given energy subband, the charge flow is written in the ballistic limit as the difference between the positive flux, corresponding to a thermoionic injection of carriers at equilibrium with the source, and the negative flux, corresponding to a thermoionic injection of carriers at equilibrium with the drain. The tunnelling current through the potential barrier is thus neglected, as well as coherence effects. To account for backscattering in the channel, a unique (let's say effective) parameter r is introduced, representing the proportion of the carriers backscattered towards their initial reservoir (source of drain) after an interaction between the virtual source and the drain. Within these assumptions, the current can be written as a function of the inversion charge density at the virtual source as:

$$I_{DS} = W \sum_{i \quad j} Q_{INV\,i,j} \cdot v_{inj\,i,j} \left(\left(\frac{1-r}{1+r} \right) \cdot \frac{1 + \dfrac{\Im_0(\eta_{Fi,j} - U_D)}{\Im_0(\eta_{Fi,j})}}{1 + \left(\dfrac{1-r}{1+r} \right) \dfrac{\Im_0(\eta_{Fi,j} - U_D)}{\Im_0(\eta_{Fi,j})}} \right) \cdot \left(\frac{1 - \dfrac{\Im_{1/2}(\eta_{Fi,j} - U_D)}{\Im_{1/2}(\eta_{Fi,j})}}{1 + \dfrac{\Im_0(\eta_{Fi,j} - U_D)}{\Im_0(\eta_{Fi,j})}} \right)$$

where W is the transistor width, $Q_{INVi,j}$ is the inversion charge density at the virtual source and $v_{inj\,i,j}$ is the carrier injection velocity, both in the jth subband of the ith valley. The third factor corresponds to the ballisticity rate (BR) at a given drain bias, and the fourth factor gives the dependency of the current with the drain bias at the ballistic limit. $\Im_{1/2}$ and $\Im_0$ are the Fermi-Dirac integrals of order ½ and 0 respectively [18] and $\eta_{Fi,j}$ is the degeneracy parameter, defined as the difference between the Fermi level and the jth subband energy level, normalised by k_BT/q. U_D is the normalised drain voltage, $U_D = V_{DS}/(k_BT/q)$ where k_B is the Boltzmann's constant and T is the temperature. Note that r represents an averaged backscattering coefficient over the different subbands and valleys.

This model can be further simplified assuming only one populated sub-band and strong carrier degeneracy. That way, Fermi-Dirac integrals simplify to power functions and the drain current expression in the saturation regime reduces to:

$$I_{DS}^{SAT} = W \frac{8}{3\sqrt{\pi}} \frac{\hbar Q_{\text{inv}}^{3/2}}{m_{\text{cond}} \sqrt{q g_0}} \frac{1-r}{(1+r)^{3/2}}$$

with m_{cond} the conductivity effective mass of the carriers in the considered sub-band and g_0 the number of equivalent valleys.

The last assumptions (one populated sub-band and strong degeneracy) are generally not verified for typical nanoscale transistor geometries and polarisations. However, for thin film devices, the positions of the energy sub-bands with respect to the bottom of the conduction band for nMOSFETs (or the top of the valence band for pMOSFETs) are almost exclusively dependent on the overall inversion charge and the transverse electrical field at the back interface whatever the geometry and the biases, as long as the silicon film is higher than 5–7 nm. Thus, we can define from Poisson-Schrödinger simulations 'universal' abaci of a corrective factor f_{sat} for the above equation, which takes into account the relative population of all the sub-bands and their corresponding level of degeneracy [19]. Then, the backscattering coefficient r can be simply estimated in the saturation regime from the experimental determination of the drain current and of the charge density at the virtual source [20] by:

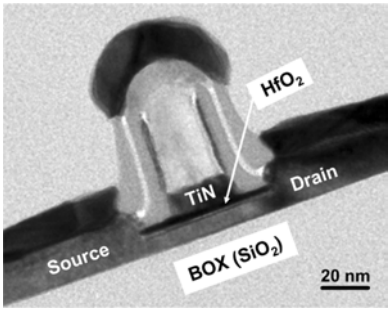
$$\frac{1-r}{(1+r)^{3/2}} \approx \frac{3\sqrt{\pi}}{8}\frac{m_{\text{cond}}\sqrt{qg_0}}{\hbar}\frac{I_{DS}^{\text{sat}}/W}{f_{\text{sat}}Q_{\text{inv}}^{3/2}}.$$

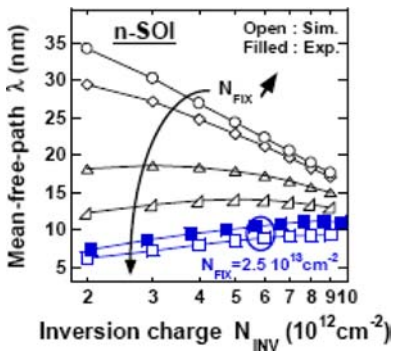
A similar analysis can be carried out in the linear regime, leading in that case to:

$$1-r \approx \frac{\hbar}{\sqrt{2g_0}}\frac{\pi}{q}\left[\frac{\left(I_{DS}^{\text{lin}}/W\right)/V_{DS}}{f_{\text{lin}}Q_{\text{inv}}^{1/2}}\right]^{3/2}.$$

From the extraction of the backscattering coefficient in the linear regime, the mean free path of carriers in transistor channels can be experimentally estimated [21]. Figure 7 shows the comparison between the mean free paths extracted from thin film FDSOI devices and calculated form the Kubo Greenwood formulation detailed above. A reasonable agreement is observed between experimental and calculated values for an inversion charge ranging from 2×10^{12} cm^{-2} to 10^{13} cm^{-2}.

Figure 7 Left: TEM cross-section of a thin film FDSOI device, featuring high-κ dielectrics, metal gate and elevated source and drain. Right: Experimental (filled symbols) electron mean free path as a function of the inversion charge vs. mean free paths obtained by simulation (open symbols) for various fixed charge densities in the gate stack. A reasonable agreement between experimental and simulated results is observed for a fixed charge density $N_{\text{fix}} = 2.5 \times 10^{13}$ cm^{-2} (see online version for colours)





3 Limits of ballistic transport in silicon nanowires

Semiconducting nanowires with diameter down to the nanometre scale can also be fabricated by catalytic growth techniques. These bottom-up nanostructures have become the subject of intense study and are considered as potential building blocks for nanoscale electronics due to their promising electronic and optical properties. Compared to classical planar technology, silicon-based semiconducting nanowires (SiNWs) are able to better accommodate 'all-around' gates, which improves field effect efficiency and device performance. Also, in contrast to many other nanowire materials, structurally stable and electrically active SiNWs can be manufactured with small diameters $d < 5$ nm.

However, as the lateral size of the nanowires becomes smaller the impact of structural imperfections such as surface disorder and defects becomes increasingly important due to the high surface to volume ratio. In the case of lithographic SiNW-FETs surface roughness disorder (SRD) is known to be a limiting factor. Moreover, due to the indirect band gap of silicon, SiNWs can be expected to exhibit fundamentally different electronic properties depending on the nanowire crystal orientation. For engineering of performant SiNW-based transistors it is thus imperative to find out how sensitive the transport properties are to SRD and which nanowire orientation is best suited for engineering highly performant transistors.

The understanding of charge transport in silicon nanowires demands for an extensive use of atomistic models (ab initio or tight-binding models). Indeed, in situation of strong geometrical and electrical confinement, electronic band structures and transport mechanisms are severely modified. The limits for ballistic transport depend on several factors owing to the fluctuations of microscopic scattering sources. For instance, scattering from impurity charges continuously vary with downsizing device features as a consequence of size-dependent screening phenomena. One of the important sources of ballistic transport is the surface roughness (SR) which is unavoidable at the atomistic scale. We have been investigating SR effects in SiNWs with diameter in the range of a few nanometres. The electronic structure of the SiNWs is described by an accurate third nearest neighbour sp^3 tight-binding (TB) Hamiltonian, previously validated by ab initio calculations and comparison with experimental data [22]. In contrast to fully ab initio approaches, the tight-binding method indeed allows quantum transport calculations on long and disordered nanowires.

Figure 8 shows a typical SR profile of our simulated nanowires, together with typical profiles observed in experiments. The surface roughness profile is characterised by the rms of the radius variations and by a correlation length L_r (the typical length scale of these fluctuations). The analysis of the roughness effect on ballistic transport has been achieved by using two complementary approaches: an order N Kubo-Greenwood method, which gives a straightforward access to the intrinsic elastic mean free paths and charge mobilities [23] and a Landauer-Büttiker approach [24] which is particularly well suited to the quasi-ballistic regime, where contact effects start to prevail over intrinsic phenomena. Both methods have been implemented numerically and extensive use of supercomputing facilities has allowed extracting quantitatively the elastic mean free path that fixes the limit for ballistic conduction. Figure 9 shows the computed charge conductivity for hole and electron as a function of charge energy or charge carrier density, and a given roughness profile defined by L_r (the typical length scale of fluctuations of the radius) [25].

Figure 8 Illustrations of surface roughness in large (a) and small diameter (c) silicon nanowires, together with description of roughness profiles at the atomic scale (b) and (d) (see online version for colours)

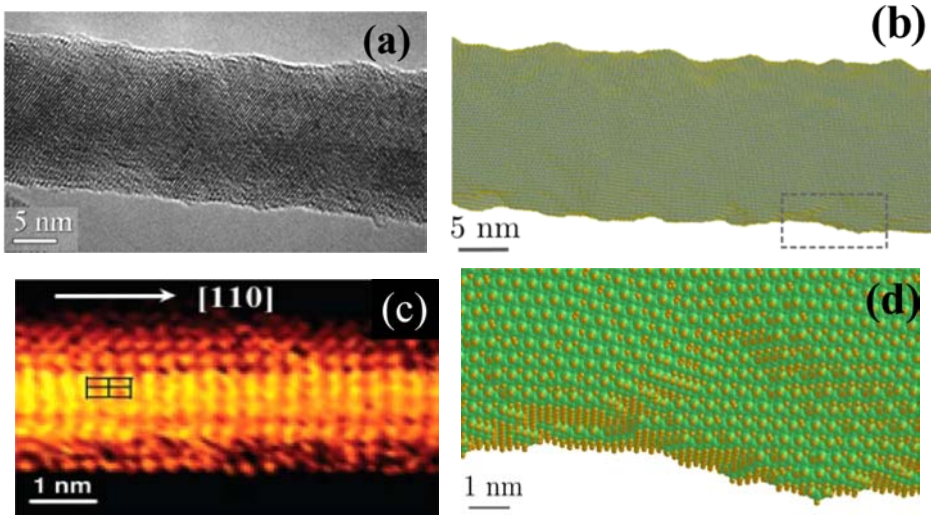
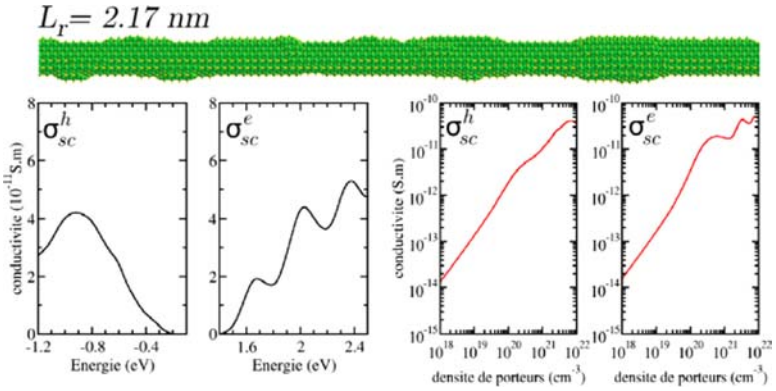


Figure 9 Top: Illustration of a small diameter SiNWs with a given roughness profile. The length scale of recurrent radius fluctuations is given by L_r (see text). Bottom: Computed charge conductivity for hole and electron as a function of charge energy or charge carrier density (see online version for colours)



The room-temperature mobility is plotted as a function of the carrier concentration on Figure 10 for ultimate SiNWs with radius $R = 1$ nm and three different orientations ([001], [110] and [111]). The rms of the radius fluctuations is $\Delta R^2 = 1$Å and the typical length scale of these fluctuations is $L_r = 2.17$ nm. As evidenced on this figure, the roughness-limited mobility is highly dependent on the nanowire orientation. Indeed, such small nanowires are in the quantum regime where only one or a few subbands are occupied and available for charge transport at room temperature. Due to the anisotropy of the band structure of bulk silicon, the electronic properties (effective masses of the electron and holes, subbands degeneracies and splittings) of the nanowires are strongly dependent on their orientation.

For example, the 6-fold degeneracy between the conduction band valleys of bulk silicon is completely lifted in [110]-oriented nanowires, which suppresses intervalley scattering at low electron energies. Moreover, the lowest subbands of these [110]-oriented nanowires exhibit a rather light (~0.15 m_0) effective mass compared to [001]- and [111]-oriented nanowires. This explains why the [110] orientation is found to be the best for electron transport. Likewise, the [111] direction is found to be the best for hole transport, because the hole mass is light in these nanowires, and because the splitting between the highest two valence subbands is the largest (~150 meV), therefore inhibiting interband scattering at low carrier concentration. The above trends are expected to hold as long as the intervalley splitting in the conduction band, or the splittings between the highest two valence bands is somewhat greater than kT, i.e., for radius $R < 3$ nm at room temperature. Quantum effects should average out beyond this radius.

For small nanowires the surface roughness will affect the charge density in an FET channel. Due to the confinement effect charges can be expected to localise in regions with locally large effective diameter. A FET was modelled using a Si nanowire with a radius of $R = 1$ nm and an 30 nm long intrinsic segment with surface roughness coupled to ideal n-doped ($n = 10^{18}$ cm^{-3}) nanowire contacts. The surface roughness is modelled in the same manner as in Lherbier et al. [25]. The nanowire channel, see Figure 11(a), is surrounded by a 30 nm all around gate (AAG), with a $t = 2$ nm HfO_2 layer insulating layer, covering the rough section of the wire. The conductance and density matrix is computed using recursive Green's function formalism, where the Hamiltonian is described by a 3rd nearest neighbour sp^3 tight binding model [22]. The charge density integral is computed as a contour integral in the complex plane, according to the residual theorem, the numerical integral is evaluated by Gaussian quadrature.

Figure 10 Computed charge mobility for hole (left) and electron (right) as a function of charge carrier density (see online version for colours)

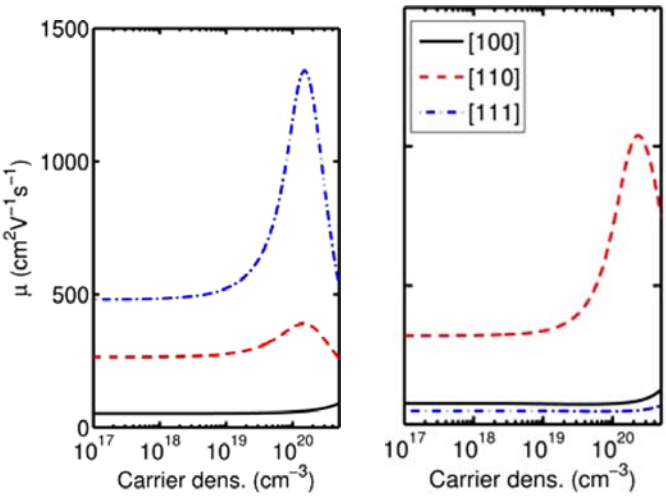
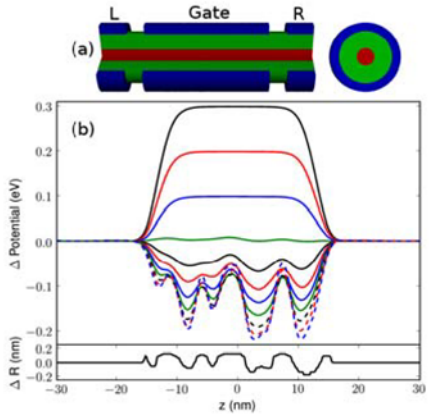


Figure 11 (a) Schematic drawing of the Si nanowire FET. (b) Electrostatic potential (top panel) at the centre of the nanowire, computed at V_{SG} = 0.3–0.7 V with steps of 0.1 V. Effective local radius (bottom panel) along the nanowire (see online version for colours)



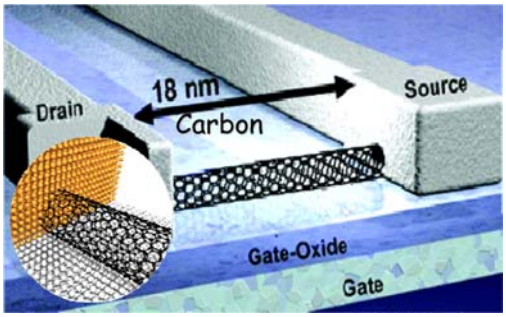
To achieve a self consistent solution for the electrostatic potential the Hamiltonian is coupled self consistently to Poisson's equation trough the charge density. Figure 11(b) show the electrostatic potential through the centre of the wire (top panel) together with the average radius of the wire (bottom panel). The gate voltage is swept from OFF to ON in the interval V_{SG} = 0.3–0.7 V in steps on 0.1 V. With the device in the OFF state, V_G = 0.3–0.1 V, the electro static potential show no correlation with the surface roughness disorder. However, as we reach the threshold voltage the potential begins to show a weak correlation with the surface roughness profile. As the gate voltage is further increased, V_G = 0.1–0.7 V, the correlation between the potential and surface roughness profile becomes more pronounced and we can clearly see that the potential increases in the sections where the average wire thickness is large while it decreases in sections with small wire thickness. Naturally we can expect the potential to have an impact on the transmission. In non self consistent studies it has been shown that surface roughness has a strong impact on the transmission for thin Si nanowires. For the FET this only remains true for gate voltages below and around the threshold voltage. As the channel is filled with charges the electrostatic potential begin to compensate for the surface roughness and we regain an almost perfect transmission. Unfortunately the transition from high to low scattering takes place over a gate voltage of about 0.2 V, so even though we regain most of the conductance the subthreshold slope for the device will be very slow.

4 Ballistic transport in carbon-nanotubes FETs

Amongst the most promising materials for the development of BEYOND CMOS nanoelectronics, carbon nanotubes [26] and graphene-based materials [27,28] and devices deserve some particular consideration. Indeed, first, their unusual electronic and structural physical properties promote carbon nanomaterials as promising candidates for a wide range of nanoscience and nanotechnology applications. Carbon is unique in possessing allotropes of each possible dimensionality and, thus, has the potential

versatility of materials exhibiting different physical and chemical properties. Diamond (3D), fullerenes (0D), nanotubes (1D-CNTs), 2D graphene and graphene ribbons are selected examples. Because of their remarkable electronic properties, CNTs or graphene-base materials should certainly play a key role in future nanoscale electronics. Not only metallic nanotubes and graphene offer unprecedented ballistic transport ability, but they are also mechanically very stable and strong, suggesting that they would make ideal interconnects in nanosized devices. Further, the intrinsic semi conducting character of other nanotubes, or graphene nanoribbons, as controlled by their topology, allows us to build logic devices at the nanometer scale, as already demonstrated in many laboratories. In particular, the combination of 2D graphene for interconnects (charge mobilities in graphene layers as huge as 400,000 $cm^2V^{-1}s^{-1}$ have been reported close to the charge neutrality point) together with graphene nanoribbons for active field effect transistor devices could allow completely carbon-made nanoelectronics.

Figure 12 Schematic drawing of the carbon-nanotube FET. The possible interface geometry between the nanotube and the metal and substrate is also illustrated (see online version for colours)

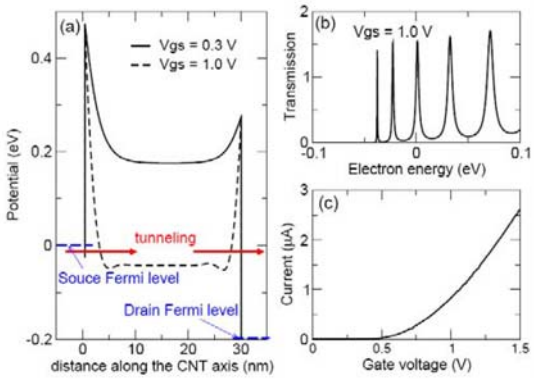


To date, the development of nanotubes and graphene science have been strongly driven by theory and quantum simulation [26,27]. The great advantage of carbon-based materials and devices is that, in contrast to their silicon-based counterparts, their quantum simulation can be handled up to a very high level of accuracy and realistic scope. The complete understanding and further versatile monitoring of novel forms of chemically-modified nanotubes and graphene will however increasingly demand for more sophisticated computational approaches, combining first principles results with advanced order N schemes to tackle with material complexity and device features, as developed in some recent literature [29].

Here we report on our recent results concerning charge transport in carbon nanotubes-based field effect transistors (an illustration is shown in Figure 12). Such devices can exist in two flavours driven by the charge injection mechanism. Indeed, depending on the nanotube geometrical features (chirality, diameter) and contact material (palladium, gold, etc.) the resulting CNTFET might operate either as an ohmic or Schottky-type field effect transistor (SB-CNTFET). Ohmic CNTFETs operate essentially like standards MOSFETs: the current is modulated by the potential barrier, inside the channel region controlled by the gate. Conversely, in SB-CNTFETs, the current is mainly modulated by the Schottky barrier widths at the metal/nanotube contacts. The barrier profiles are controlled by a gate electrode, and the current in the ON state comes essentially from tunnelling through the source barrier, which is a

purely quantum phenomenon (as illustrated in Figure 13). Ohmic transistors are obtained for nanotubes with diameter as large as 2–3 nm with palladium or platinium contact, whereas SB-CNTFET are found for nanotube diameter in the order of 1 nm. If SB-CNTFET are in principle more difficult to control, owing to the sensitivity of charge injection ate the contact to environmental factors, their performances turn out however to overcome ohmic-based CNTFETs. An important issue is to understand the connection between a given nanotube/metal contact and the resulting Schottky barrier features. This was pointed out by Tersoff [30] early on, who emphasised on the need of first principles calculations.

Figure 13 Simulation of a SB-CNTFET using the NEGF technique. The transistor channel is a 30 nm long semiconducting nanotube of helicity (10,0). The all-around cylindrical gate is at a distance of 1.5 nm from the nanotube. The source-drain voltage V_{ds} is set to 0.2 Volts. (a) Conduction band diagrams for two values of the gate voltage V_{gs}. The Schottky barriers widths decrease as V_{gs} increases. Once the width is small enough (a few nm), electrons can tunnel through the barriers. (b) Transmission spectrum at V_{gs} = 1 V, for energies around the source Fermi level. The peaks are due to the discrete energy levels in the quantum well formed in the channel between the two barriers. (c) Source-drain current vs. gate voltage (see online version for colours)



To simulate CNTFETs, we use the Non Equilibrium Green's Functions (NEGF) technique, which fully takes into account the quantum phenomena occurring in these nano-sized systems. The technique consists in solving the Schrödinger equation with the Green's function formalism, which gives the electrical current and the charge distribution in the system connected to two electrodes. The Schrödinger equation is coupled self-consistently with the Poisson equation to take into account the electrostatic environment (electrodes and dielectric materials). Since CNTFETs are small systems, it is possible to refine the models without increasing too much the computing time. For instance, it is possible to consider tight-binding Hamiltonians with several orbitals on each atom. It is also possible to include impurities, grafted molecules (see [31]), or more realistic descriptions of metal/nanotube contacts. The NEGF technique is particularly well suited for SB-CNTFETs, since the electron tunnelling through the Schottky barriers requires a quantum treatment. In Figure 13, we show simulation results for a SB-CNTFET with an all-around cylindrical gate. The nanotube channel is described by a simple one orbital tight-binding model, and the nanotube contacts are also modelled in a simple manner. Work is in progress to improve the modelling of metal/nanotube contacts, using first principle calculations.

5 Conclusion and perspectives

To conclude, we have presented several approaches to tackle charge transport in nanometre-sized field effect transistors, including silicon nanowires and carbon nanotubes based devices. Part of these efforts targets the bridging of advanced ab initio/atomistic computational approaches to ultimate high-level simulation tools such as TCAD models. The presented computational methodologies have included Kubo-Greenwood approach for computing charge mobilities, and non-equilibrium Green functions that give a more suitable framework for device simulation in a quantum regime.

Many fields such as organic electronics, spintronics, beyond CMOS nanoelectronics, nanoelectromechanical devices, nanosensors, nanophotonics devices genuinely lack standardised and enabling tools, that are however mandatory to assess the potential of new concepts, or to adapt processes and architectures to achieve the desire functionalities. The multiscale computational methodologies developed in CEA are versatile enough to explore those novel physical phenomena that require advanced quantum mechanics, while at the same time strong efforts are devoted to reach high level of predictability efficiency, therefore providing guidance for experiments and technology.

Acknowledgements

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