Double magnetic tunnel junctions suitable for automotive memory applications

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Stage pouvant se poursuivre en thèse : Oui

Résumé :

There is an increase interest in microelectronics industry for a new type of magnetic non-volatile memory called STT-MRAM. In these memories the storage elements are magnetic tunnel junctions which consist of two ferromagnetic layers separated by a thin tunnel oxide barrier (MgO). They are about to be introduced in products for consumer electronics. It is envisioned that they could play also a very important role in industrial and automotive applications but for the latter, the specifications are much more stringent in terms of reliability and operating temperatures (up to 150°C instead of 80°C for consumer electronics). In this internship and possibly the subsequent thesis project, we propose to explore several routes allowing to increase the performances of these memories in terms of switching speed, power consumption and operating range.

Sujet détaillé :

The advent of STT-MRAM in microelectronics industry represent a major breakthrough which will significantly contribute to reducing the power consumption of electronic circuits. STT-MRAM are non-volatile memories based on magnetic tunnel junctions (MTJ). MTJ consist of two ferromagnetic layers separated by a very thin MgO tunnel barrier (1nm thick). The information is encoded in the magnetic orientation of one of the layer (called storage layer) while the magnetization of the other layer remains fixed. When a current flows through the junction, the resistance depends of the relative orientation of the magnetization of the two magnetic layers (Parallel=?0?=low resistance state; antiparallel=?1?=high resistance state). During write, the magnetic state of the storage layer is switched by a phenomenon called spin transfer torque which results from the exchange interaction between the spin of the tunneling electrons and those responsible for the magnetization of the storage layer. SPINTEC played a leading role in the development of magnetic memories based on these structures which are now about to be widely adopted by the microelectronic industry. For some applications, further work is however still needed to increase the switching speed (to reach the ns regime with high reliability), to reduce the write current for downsize scalability and to increase the temperature operating range.

In this internship, we propose to study double barrier magnetic tunnel junctions with double polarizers. Compared to the structures developed so far, those should have higher performances in terms of thermal stability of the storage layer magnetization against thermal fluctuations (i.e. improved memory retention) and larger spin transfer torque efficiency allowing lower write current. Based on the previous experience of our laboratory, we propose to grow this type of stacks by sputtering, characterize their magnetic properties as well as their electrical properties at wafer level. We will then pattern the stacks in the form of nanometric pillars in our clean room and characterize their switching by spin transfer torque. The results will be benchmarked with the properties of the existing structrues.

We hope that the internship will be pursued in a thesis. This would allow a thorough optimization of the stack to reach specifications compatible for automotive and industrial applications

Compétences requises :

Basics in magnetism, solid state physics, nanosciences, nanotechnology